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Dynamic Power Reduction in Digital VLSI Circuits Using Stacked LCNMOS.

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ABSTRACT

In deep submicron technologies, leakage power becomes a key for a low power design due to its ever increasing proportion in chips total power consumption. Power dissipation is an important consideration in the design of CMOS VLSI circuits. High power consumption leads to reduction in battery life in case of battery powered applications and affects reliability packaging and cooling costs. We propose a technique called Stacked LCNMOS for designing CMOS gates.

LCNMOS technique significantly cuts down the leakage current without increasing switching power dissipation. LCNMOS, a technique to tackle the leakage problem in all digital circuits, uses single additional Leakage Control Transistor (LCT) driven by the output from the pull up and pull down networks, which is placed in a path from pull down network to ground. This LCT provides the additional resistance thereby reducing leakage current in path from supply to ground. In stacked LCNMOS technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width. It overcomes the limitation of sleep technique by retaining states. All the performances has been investigated using 90nm technology at one voltage and evaluated by the comparison of the simulation result obtained from T-SPICE.

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Introduction:

The main sources for power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub threshold currents. The former is due to the stored charge between the drain and bulk of active transistors while the latter is due to the carrier diffusion between the source and drain of the OFF transistors as shown in fig1.

Digital integrated circuits are found everywhere in modern life and many of them are embedded in mobile devices where limited power resource is available (e.g. mobile phones, watches, mobile computers…). To permit a usable battery runtime, such devices must be designed to consume the lowest possible power. Furthermore, low power is also very important for non-portable devices, too. Indeed reduced power consumption can highly decrease the packaging costs and highly increase the circuit reliability, which is tightly related to the circuit working temperature. Hence, low power consumption is a zero-order constraint for most ICs manufactured today. In fact, higher performance-per-watt is the new mantra for micro-processor chip manufacturers today. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially. The reduction of the supply voltage is dictated by the need to maintain the electric field constant on the ever shrinking gate oxide. Unfortunately, to keep transistor speed (proportional to the transistor "on" current) acceptable, the threshold voltage must be reduced too, which results in an exponential increase of the "off" transistor current, i.e. the current constantly flowing through the transistor even when it should be "non-conducting".

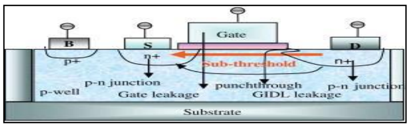

Fig. 1: Static CMOS leakage sources.

As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor increases when it is off as shown in fig. 2 Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e. leakage power dissipation has become a significant portion of total power consumption for current and future silicon technologies .To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above.

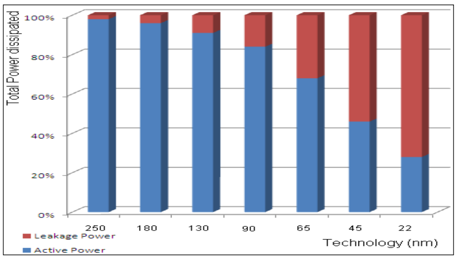

Fig. 2: Technology Vs Leakage Power

In this paper, we describe a new leakage power reduction technique called LCPMOS (Leakage Control PMOS) for designing CMOS circuits. The rest of the paper is organized as follows. Section II describes briefly the prior works on leakage power reduction and their limitations. Section III introduces the transistor models used for estimating the leakage power. Our design strategy and an approach for minimizing the area overhead are described in Sections IV. Results are presented in Section V, followed by conclusions in Section VI respectively.

Limitations with related work:

A. MTCMOS

A high-threshold NMOS gating transistor is connected between the pull-down network and the ground, and low-threshold voltage transistors are used in the gate. The reverse conduction paths exist, which tends the noise margin to reduce or may result in complete failure of the gate. There also exists a performance penalty due to the high-threshold transistors in series with all the switching current paths.

Dual V_T technique is a variation in MTCMOS, in which the gates in the critical path use low-threshold transistors and high-threshold transistors for gates in non-critical path [3], [7]. Both the methods requires additional mask layers for each value of V_T in fabrication, which is a complicated task depositing two different oxides thickness, hence making the fabrication process complex. The techniques also suffer from turning-on latency i.e., the idle subsections of circuit cannot be used immediately after reactivated since some time is needed to return to normal operating condition. The latency is typically a few cycles for former method, and for Dual technology, is much higher. When the circuit is active, these techniques are not effective in controlling the leakage power.

B. SLEEP Transistor Technique

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull-down networks and gnd while for fast switching speeds, low-Vth transistors are used in logic circuits [8]. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

C. Forced Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width [6]. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time

D. ZIGZAG Technique

Wake-up cost can be reduced in zigzag technique but still state losing is a limitation. Thus, any particular state which is needed upon wakeup must be regenerated somehow. For this, the technique may need extra circuitry to generate a specific input vector.

E. SLEEPY STACK Technique

This technique combines the structure of the forced stack technique and the sleep transistor technique. In the sleepy stack technique, one sleep transistor and two half sized transistors replaces each existing transistor [10]. Although using of W0/2 for the width of the sleep transistor, changing the sleep transistor width may provide additional tradeoffs between delay, power and area. It also requires additional control and monitory circuit, for the sleep transistors.

F. LEAKAGE FEEDBACK Technique

This technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

G. SLEEPY KEEPER Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to V_{dd} and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active [9]. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state.

H. LECTOR Technique

This technique consists of two self-controlled transistors which increase the resistance in the path from source to ground, which increases the area of the circuit, one of the most important constraints in the design of VLSI circuits.

LCPMOS:

In this proposed technique, we introduce a single leakage control transistor within the logic gate for which the gate terminal of leakage control transistor (LCT) is controlled by the output of the circuit itself which increases the resistance of the path from pull down network to ground thereby increasing the resistance from Vdd to ground, leading to significant decrease in leakage currents. The main advantage as compared to other techniques is that LCPMOS technique does not require any additional control and monitoring circuitry, thereby limits the area and also the power dissipation in active state.

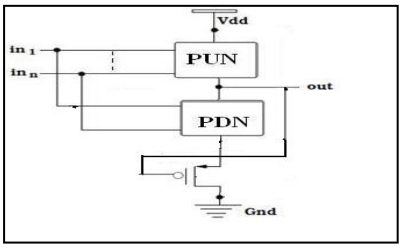

Fig. 3: LCPMOS CMOS Gate

LCNMOS:

One Leakage Control Transistor (LCT), is introduced between pull down network and ground. The gate terminal of LCT is controlled by the output of circuit itself. No external control circuitry is required using the LCNMOS implementation. The introduction of LCT increases the resistance of the path from pull down network (PDN) to Gnd, which increases the resistance from Vdd to Gnd, thereby reducing leakage.

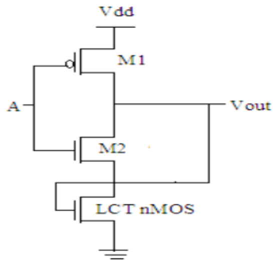

Fig. 4: LCNMOS based CMOS Gate

STACKED LCNMOS:

The basic idea behind this approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. We initially had LCNMOS technique, from which STACKED LCNMOS is derived. This is based on the observation that "a state with one transistor OFF in a path from supply voltage to ground is far less leaky." In LCNMOS technique one leakage control transistor (one n-type) is introduced between pull-down and ground circuit within the logic gate for which the gate terminal of leakage control transistor (LCT) is controlled by the output of the circuit itself.

In this technique, we implement LCNMOS and STACKED technique together. In this, we duplicate every single transistor and replace the original transistor with two transistors each having half the width of original transistor.

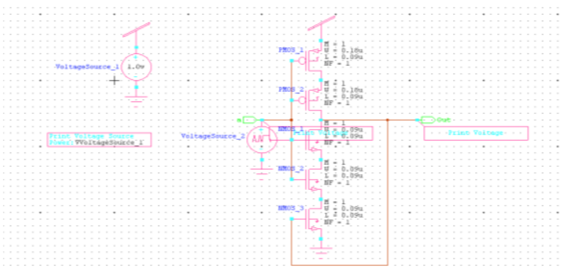

Fig. 5: Stacked LCNMOS NOT Gate

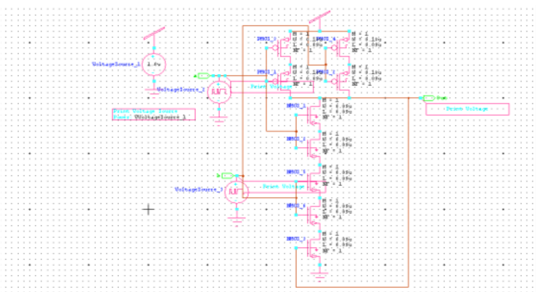

Fig. 6: Stacked LCNMOS NAND Gate

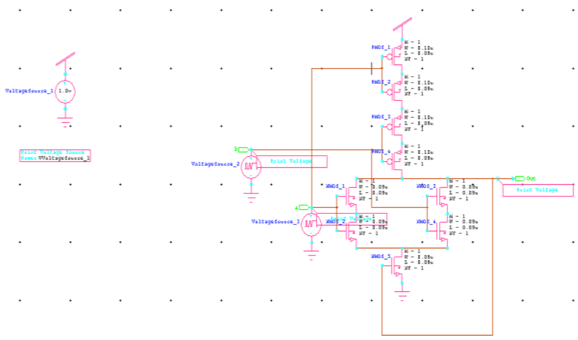

Fig. 7: Stacked LCNMOS NOR Gate

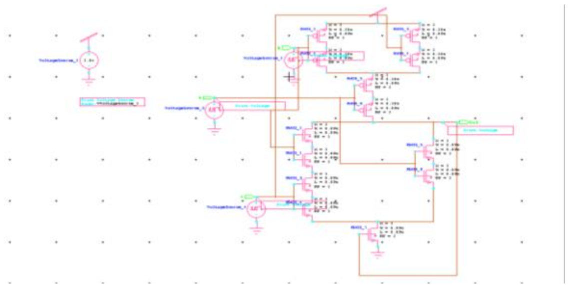

Fig. 8: Stacked LCNMOS AOI Gate

Table: 1. Power consumption of different techniques

Technology (90nm) GATES	Leakage Power In Micro Watt (µw)			
	NOT (µw)	NAND (µw)	NOR (µw)	AOI (µw)
BASE CAE	5.36	5.42	3.57	6.27
LECT OR	4.23	4.71	2.73	5.48
LCN MOS	4.34	4.44	2.58	4.59
STACKED LCN MOS	4.21	1.5	1.92	3.91

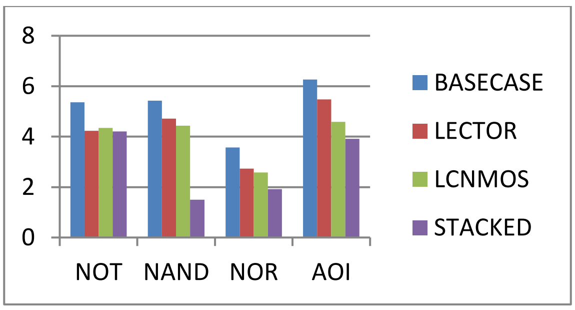

Fig. 9: Bar graph representation

Conclusion:

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this thesis, we present a new circuit structure named "STACKED LCNMOS" to tackle the leakage problem. STACKED LCNMOS yields better leakage reduction as the threshold voltage decreases and hence aids in further reduction of supply voltage and minimization of transistor sizes. STACKED LCNMOS uses one additional transistor. Compared to other leakage reduction techniques, like LECTOR, sleepy stack, sleepy keeper, etc, STACKED LCNMOS achieves leakage power reduction but with the advantage of not effecting the dynamic power as this technique does not having any additional control and monitoring circuitry like in sleep techniques and it also maintains exact logic state.

The STACKED LCNMOS technique can retain logic state, so it can be used for both generic logic circuits as well as memories, i.e., SRAM. When applied to generic logic circuits, the STACKED LCNMOS technique achieves up to 85-90% leakage reduction over the conventional circuits without affecting the dynamic power.

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